

REMARKS

The 25 February 2005 official action addressed claims 1-20.

1. Overview of amendments

Drawings amendments

Figure 4 is amended to be labeled as "Prior Art."

Figure 5d is amended to replace the reference numeral 59 with the reference numeral 61, consistent with the specification at page 9, paragraph 23.

No new matter is added.

Claim amendments

Claim 5 is canceled.

No new matter is added.

2. Response to objections and rejections

Drawing objections

The amendments to the drawings overcome the objections noted in the official action.

Claim objection

Claim 5 is canceled.

Prior art rejections

Claims 1-20 were rejected under 35 USC §103(a) as being obvious over Nakaoka (U.S. 6,337,500) in view of Baba (U.S. 6,852,604). It is believed that the claims are distinguished from the cited references for the reasons that follow.

The invention described in independent claims 1 and 20 involves the formation of point defects in a silicon germanium layer of a strained silicon MOSFET structure that retard the diffusion of n-type dopants during annealing. In this structure, a strained silicon layer is formed on a silicon germanium supporting layer, and point defects are formed in the silicon germanium by implantation of a species at any of various points in the fabrication process (see claims 2-4 and 6-9).

Nakaoka teaches a process for fabricating a silicon on insulator (SOI) MOSFET. In this structure, a silicon region is formed on an insulating layer. Referring to Nakaoka's Figure 4b, the silicon region 303 is surrounded on all sides by a silicon oxide layer 302 and silicon oxide isolations 304 (the processing at figure 6(b) and 7(b) involve similar SOI structures). Nakaoka implants a p-type impurity into the silicon region 303 to produce a high concentration region 316 and a defect region 315. The purpose of the defect region 315 is explained in Nakaoka's summary:

[T]he present invention provides a region for eliminating carriers in the vicinity of the channel region of the SOI transistor such as a lattice defect region containing a lot of lattice defects functioning as the center of recombination, ... Col. 2, line 65 – col. 3, line 2.

[W]hen hole-electron pairs are generated in the channel region during the operation of the semiconductor device, the holes gather in parts of the channel region in the vicinity of the source/drain regions or in the source/drain regions. However, the holes are soon eliminated because the hole-eliminating region is provided to be adjacent to the channel region and either the source region or the drain region. Consequently, no bipolar operation results from the accumulation of holes, thereby maintaining the source/drain breakdown voltage at a high level. Col. 3, lines 18-27.

In the semiconductor device, the hole-eliminating region may be a lattice defect region formed by introducing a lattice defect to be a center of recombination. Col. 3, lines 51-53.

In other words, the point defects created by Nakaoka are provided to eliminate *carriers* (holes) that can cause bipolar operation in an SOI MOSFET. Nakaoka does not suggest that the point defects should be created to retard dopant *atoms* during annealing to prevent diffusion of those atoms, and in fact Nakaoka has no need to prevent dopant diffusion, since Nakaoka's silicon region 303 is surrounded by insulating silicon oxide structures 302, 304 that already prevent diffusion. Thus Nakaoka does not create point defects for the purpose of retarding dopant diffusion.

Further, Nakaoka does not create point defects in the source region of the MOSFET. Rather, Nakaoka creates point defects at the bottom of the active region 303. Thus the point defects would not constrain dopant diffusion to a source region, but rather dopant would be free to diffuse anywhere in the active region.

Applicants therefore submit that Nakaoka does not teach the creation of point defects around source regions to retard dopant diffusion during annealing.

Baba teaches a strained silicon MOSFET in which a strained silicon layer is supported on a silicon germanium layer. Baba does not address the dopant diffusion issue.

There is no motivation to combined Nakaoka and Baba. Nakaoka describes a process that eliminates a problem found in silicon on insulator MOSFETs. Baba does not involve silicon on insulator MOSFETs and so one would not find Nakaoka's teachings to be relevant to Baba and would not implement them in Baba.

Consequently the process specified by independent claims 1 and 20 and their dependent claims does not follow from the teachings of Nakaoka and Baba.

Further, with regard to dependent claims 17 and 18, neither reference teaches an annealing process in which the annealing time is constrained to a transient region that has been extended through the creation of point defects as recited. In regard to these features, the reasoning in the final sentence of the final paragraph at page 8 of the official action is not understood. The official action

states that "there would be less duration time needed to perform the diffusion of the dopant materials." Applicant submits that a better understanding is that the point defects extend the duration of the transient region, thus allowing longer annealing periods while still remaining in the transient region. Reconsideration in light of these comments is requested.

The foregoing amendments and remarks address all bases for objection and rejection and are believed to place the case in condition for allowance. The examiner is invited to contact the undersigned to resolve any remaining issues.

Respectfully submitted,

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By

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